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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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R C van Dijk

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
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Array of cells including a selection bipolar transistor and fabrication method thereof

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ARRAY OF CELLS INCLUDING A SELECTION BIPOLAR TRANSISTOR AND FABRICATION METHOD THEREOF

The present invention relates to an array of cells including a selection bipolar transistor and a fabrication method thereof. In particular, the invention refers to a cell array of a phase change memory (PCM) device, without being limited thereto.

As is known, phase change memory cells utilize a class of materials that have the unique property of being reversibly switcheable from one phase to another with measurable distinct resistivity. Specific materials that may be suitably used in phase change memory cells are alloys of elements of the VI group of the periodic table as Te or Se, also called chalcogenides or chalcogenic materials. Thus a thin film of chalcogenic material may be employed as a programmable resistor, switching between a high and a low resistance condition.

The use of chalcogenic storage elements has been already proposed to form a memory cell. To avoid disturbances caused by adjacent memory cells, the chalcogenic element is generally coupled with a selection element, generally a MOS transistor or a diode.

A possible organization of a PCM array is shown in Figure 1. The memory array 1 of Figure 1 comprises a plurality of memory cells 2, each including a storage element 3 of the phase change type and a selection element 4 formed as a bipolar PNP transistor. The same architecture may be however used for any array of storage elements that are selectively addressed through respective bipolar transistor selection elements.

The memory cells 2 are arranged on rows and columns. In each memory cell 2, the storage element 3 has a first terminal connected to an own bit line BLn-1, BLn, BLn+1, ..., and a second terminal connected to an emitter of an own bipolar transistor 4; the bipolar transistor 4 has a base connected to an own control line, also called word line WLn-1, WLn, WLn+1, ... and a grounded collector.

In order to address the storage element 3 belonging to a specific cell 2, for example the one connected to bit line BLn and to world line WLn, the bit line connected to the addressed cell (selected bit line BLn) is biased at a high voltage V_{OP} and all the other (unselected) bit lines BLn-1, BLn+1, ... are grounded. Furthermore, the word line connected to the addressed cell (selected word line WLn) is grounded and all the other (unselected) word lines WLn-1, WLn+1, ...

are biased at V_{CC}, so that the bipolar transistors 4 not connected to the selected word line are held off.

CMOS compatible processes for manufacturing PCM have been already proposed. For example, European patent application N. 01128461.9 filed on 5.12.2001 describes a process providing a small area contact between the chalcogenic region and the resistive electrode. In this prior patent application, each cell is housed in an own active area. This prior application however does not deal with the optimization of the layout of the memory cell.

Since electronic devices are required to be more and more compact, it is desired to provide a highly compact layout for the array structure of Figure 1.

According to the present invention, there are provided a cell array and the fabrication method thereof, as defined respectively in claims 1 and 15.

To increase the compactness of the array, according to one aspect of the invention, at least two cells are housed in a same active area of the device.

In particular, according to an embodiment, strips of active area are provided, each strip housing a plurality of emitter regions and base contact regions of a plurality of selection bipolar transistors, with the emitter regions and the base contact regions

arranged alternately.

According to another embodiment, each active area has a rectangular shape and houses at least one base contact region and two emitter regions, so that at least two cells are arranged in the same active areas.

According to a further embodiment, strips of active area are provided, each strip housing a plurality of emitter regions and base contact regions of a plurality of selection bipolar transistors, at least two emitter regions being arranged between two subsequent base contact regions.

For the understanding of the present invention, preferred embodiments are now described, purely as non-limitative examples, with reference to the enclosed drawings, wherein:

- Figure 1 is a circuit diagram of an array of cells including a storage element and a selection bipolar transistor;

- Figure 2 shows the masks used for a cell array according to a first embodiment of the invention;

- Figure 3 shows a cross-section of the first embodiment, taken along line III-III of Figure 2;

- Figure 4 shows a cross-section of the first embodiment, taken along line IV-IV of Figure 2;

- Figure 5 shows the masks used for a cell array

according to a second embodiment of the invention;

- Figure 6 is a cross-section of the second embodiment, taken along line VI-VI of Figure 5;

- Figure 7 shows the masks used for a cell array according to a third embodiment of the invention; and

- Figure 8 is a cross-section of the third embodiment, taken along line VIII-VIII of Figure 7.

According to the embodiment of Figures 2-4, a memory array is formed in a body 10 of semiconductor material including a P-type common collector region 11. As visible in particular from Figure 4, the body 10 houses a plurality of active area strips 12, of N-type, defining base regions. The active area strips 12 extend parallel to each other along a first direction (X-direction) and are electrically insulated from each other by field oxide regions 13 (Figure 4).

Each active area strip 12 accommodates a plurality of emitter regions 14, of P^+-type, and plurality of base contact regions 15, of N^+-type, that are arranged alternately, that is each emitter region 14 is arranged between two base contact regions 15, and each base contact region 15 is arranged between two emitter regions 14. Thus, each pair of regions including an emitter region 14 and the adjacent base contact region 15 (for example, an emitter region 14 and the base

contact region 15 arranged on right thereof), the active area strip 12 they are accommodated in, and the underlying collector region 11 form a selection transistor 20 of PNP-type, corresponding to bipolar transistor 4 of Figure 1.

A dielectric region 21 extends on the body 10 and accommodates contacts, storage elements and interconnection lines. The dielectric region 21 is generally formed by more layers deposited subsequently to allow forming the various regions therein and may also include different materials.

First and second contacts 22, 23 extend in first and second openings 27a, 27b of the dielectric region 21. Preferably, the first and second contacts 22, 23 are of tungsten, covered on the vertical and bottom sides with a barrier material (for example, Ti/TiN), not shown for simplicity.

The first contacts 22 extend each from an emitter region 14 to a chalcogenic storage element 24 forming the storage element 3 of Figure 1. First metal lines 25, forming bit lines corresponding to bit lines BLn-1, BLn, BLn+1 of Figure 1, extend along a second direction (Y-direction), thus transversely to the active area strips 12. Each first metal line 25 is in contact with the chalcogenic storage elements 24 that are aligned in

the Y direction, as visible from the cross-section of Figure 4. The first metal lines 25 are formed preferably in a first metal level.

The second contacts 23 are higher than the first contacts 22 and extend each from a base contact region 15 to second metal lines 26. The second metal lines 26, forming word lines corresponding to word lines WLn-1, WLn, WLn+1 of Figure 1, extend along the first direction (X-direction), thus parallel to the active area strips 12 and perpendicular to the first metal lines 25. Each second metal line 25 is in contact with the second contacts 23 that are aligned in the X direction, as visible from the cross-section of Figure 3. The second metal lines 26 are formed preferably in a second metal level.

Figure 2 shows some masks to be used for manufacturing the memory array of Figures 3 and 4. In particular, Figure 2 shows an active area mask 30, a contact mask 31 and an emitter mask 32.

The process for manufacturing the memory array of Figures 3 and 4 is the following.

Initially, the field oxide regions 13 are grown in the body 10, preferably including a substrate and an epitaxial layer of P type, using the active area mask 30 of Figure 2, and thus defining the active area

strips 12.

Then the active area strips 12 are implanted with N-type doping agents, thus forming the base regions of bipolar transistors. The body 10 is covered by a first layer of insulating material, forming the bottom portion of the dielectric region 21, and contacts are opened using contact mask 31, forming the first openings 27a and the bottom portion of the second openings 27b. Then, a boron implant (P+ emitter implant) is made, using emitter mask 32, so as to form emitter regions 14 below the first contacts 22. Thereafter, using an own mask not shown, that is the negative of the emitter mask 32, base contact regions 15 are implanted below the second contacts 23. In case, the base contact regions 15 may be doped before the emitter regions 14.

Then the first openings 27a and the bottom part of the second openings 27b are filled with a barrier layer, e.g. Ti/TiN, and with tungsten; then chalcogenic storage elements 24, the first metal lines 25, the second metal lines 26, the upper portion of the dielectric region 21 and the upper portion of the second contacts 23 are formed, e.g. as described in the before mentioned European patent application N. 01128461.9.

Alternatively, instead of the chalcogenic storage elements 24, other storage elements or other two or three-terminal elements that are compatible with standard CMOS back-end processes may be formed.

According to a different embodiment, a doped region 28 of N type, having a doping level close to that of the active area strips 12, is formed below each emitter region 14, as shown by broken lines in Figure 3. In this case an N-type conductivity determining agent is implanted using the emitter mask 32, just after or just before the P+ emitter implant. Thereby, the base resistance and thus the emitter-to-base voltage drop are reduced, increasing also the immunity of the bipolar transistor against emitter-to-collector leakage and punch-through.

The embodiment of Figures 2-4 has the following advantages. First, the cell array has a very compact layout, thus reducing the overall dimensions of the device comprising the array. Furthermore, no active area corners are present inside the array, thus reducing to a minimum the stress due to isolation. There is also an intrinsic redundancy of the base contacts; the solution ensures both reduced defects and reduced intrinsic current leakage; thus the array has very good electronic properties.

Figures 5 and 6 show a different embodiment, wherein, in the X-direction, each emitter region 14 is separated by the adjacent emitter regions 14 by a base contact region 15 on one side (left in the drawings), and by a field oxide region 40 on the other side (right in the drawings). Here, the active area mask 41 (Figure 5) has an grid-like pattern, and a field oxide region 40 having a grid-like shape, delimits a plurality of active regions 42 of rectangular shape. Each active region 42 accommodates only one base contact region 15 and two emitter regions 40, arranged on different sides of the base contact region 15 in the X-direction. Thus, each active region 42 accommodate two bipolar transistors 43 that share a same base contact region 15.

The cross-section in a plane perpendicular to that of Figure 6 is the same as in Figure 4.

As visible from Figure 5, the shape of the active area mask 41 and of the emitter mask 44 differ from the active area mask 30 and the emitter mask 32 of Figure 2; however, contact mask 31 is about the same as in Figure 2.

The manufacturing process of the memory array of Figures 5 and 6 is the same described above with reference to Figures 2-4, with the only exception of

the shape of the active area mask 41 and the emitter mask 44, as above outlined.

Also in the embodiment of Figures 5 and 6 a N-doped region 28 (not shown) may be provided below each emitter region 14, to reduce the base resistance.

With the embodiment of Figures 5 and 6, it is possible to save around 20% of silicon area with respect to the embodiment of Figures 2-4, even if the active area corners could introduce defectivity issues.

Figures 7 and 8 show a third embodiment, wherein adjacent emitter regions 14 are not separated by other formations (base contacts or insulating material), but their electrical separation is only ensured by the intrinsic base region (active area strips 12).

Specifically, here the active areas are formed as active area strips 12, analogously to the embodiment of Figures 2-4, but each base contact 15 is formed every two emitter regions 14, analogously to the embodiment of Figures 5 and 6. Thus, each base contact region 15 forms two bipolar transistors 50 with the adjacent emitter regions 14.

The masks used to obtain the structure of Figure 8 are shown in Figure 7: as may be noted, the active area mask 30 is the same as in Figure 2 and the emitter mask 44 is the same as in figure 5.

The manufacturing process of the memory array of Figures 7 and 8 is the same described above with reference to Figures 2-4, with the only exception of the shape of the emitter mask 44, as above outlined.

In the embodiment of Figures 7 and 8, it is possible to further reduce the area occupation, depending on the minimum distance attainable between two adjacent emitter regions 14; however, the presence of lateral parasitic PNP bipolar transistors (formed by two adjacent emitter regions 14 and the intermediate portion of the respective active area strip 12) renders this embodiment applicable only to solutions including design measure to reduce the resulting leakage current.

According to a different embodiment, more than two emitter regions 14, e.g. four, eight, etc., may be arranged between consecutive base contact regions 15 without an oxide or base isolation between them. In this case, the area occupation is still reduced, but the current leakage problem is worsened and base resistance could become a limiting factor for the emitters located farther from the base contact.

The advantages of the present invention are clear from the above.

Finally, it is clear that numerous variations and modifications may be made to the cell array as

described and illustrated herein, all falling within the scope of the invention as defined in the attached claims.

E.g., it is possible to arrange multiple emitter regions 14 at each side of a base contact region 15 also in the embodiments of Figures 2-4 and 5-6, thus reducing the area occupation, while worsening current leakage due to parasitic components.

Furthermore, as indicated, the same array layout may be used for cells including a different storage component.

CLAIMS

1. A cell array (1) comprising a plurality of cells (2), each cell including a selection bipolar transistor (4) and a storage component (3), each said bipolar transistor (4) having a first (14), a second (11) and a control region (12, 15; 42), and each said storage component (3) having a first and a second terminal, said first region (14) of each bipolar transistor being connected to said first terminal of a respective storage component, said cell array comprising a body (10) of semiconductor material including:

a common region (11) of a first conductivity type, forming said second regions;

a plurality of active area regions (12; 42) of a second conductivity type and a first doping level, overlying said common region (11) and forming said control regions;

a plurality of conduction regions (14) of said first conductivity type formed in said active area regions and forming said first regions;

and a plurality of control contact regions (15) of said second conductivity type and a second doping level, higher than said first doping level, formed in said active area regions (12; 42),

wherein each active area region is shared by at least two bipolar transistors (20; 43; 50).

2. A cell array according to claim 1, wherein said active area regions (12) have a strip-like shape and accommodate each a plurality of conduction regions (14) and a plurality of control contact regions (15).

3. A cell array according to claim 2, wherein said conduction regions (14) and said control contact regions (15) are alternated, and each conduction region (14) is arranged between two consecutive control contact regions (15), and each control contact region (15) is arranged between two consecutive conduction regions (14).

4. A cell array according to claim 2, wherein each control contact region (15) has at least two consecutive conduction regions (14) on each side.

5. A cell array according to any of claims 2-4, comprising a plurality of insulating regions (13) having strip-like shape and extending each between two adjacent active area regions (12).

6. A cell array according to claim 1, wherein said active area regions (42) have a rectangular shape and accommodate each at least two conduction regions (14) and one control contact region (15).

7. A cell array according to claim 6, wherein said

control contact region (15) is arranged between said conduction regions (14).

8. A cell array according to claim 6 or 7, comprising an insulating region (40) having a grid-like shape accommodating said active area regions (42).

9. A cell array according to claim 8, wherein said active area regions (42) have rectangular shape and are arranged according to a matrix.

10. A cell array according to any of the preceding claims, comprising a dielectric region (21) on top of said body (10); a plurality of first and second electrical contact regions (22, 23) extending through said dielectric region (21), each said first contact region (22) extending between and contacting a respective conduction region (14) and the first terminal of a respective storage element (3), each said second contact region (23) extending from and contacting a respective control contact region (15).

11. A cell array according to claim 10, wherein said dielectric region (21) accommodates a first and a second plurality of conductive lines (25, 26), the conductive lines (25) of said first plurality extending on top of said cells (2) parallel to each other along a second direction (Y), the conductive lines (26) of said second plurality extending on top of said first

plurality, parallel to each other along a first direction (X) transverse to said second direction, the conductive lines (25) belonging to one of said first and second plurality of conductive lines being in contact with said second terminals of said storage components (3) and the conductive lines (26) belonging to another one of said first and second plurality of conductive lines being in contact with said second contact regions (23).

12. A cell array according to any of the preceding claims, wherein said storage component (3) is a phase change memory element (24) of chalcogenic material.

13. A cell array according to any of the preceding claims, wherein said first region (14) is an emitter region, said second region (11) is a collector region and said control region (12; 42) is a base region.

14. A cell array according to any of the preceding claims, comprising enriched regions (28) having said second conductivity type and a third doping level higher than said first doping level, said enriched regions extending in said active area regions (12; 42) and being located each below a conductive region (14) of a respective bipolar transistor (20; 43).

15. A process for manufacturing a cell array (1) comprising the steps of:

providing a body (10, 11) of semiconductor material of a first conductivity type;

forming a plurality of active area regions (12; 42) of a second conductivity type and a first doping level;

forming, in each active area region, at least one control contact region (15) of said second conductivity type and a second doping level, higher than said first doping level;

forming, in each active area region, at least two conduction regions (14) of said first conductivity type, each said conduction region forming, together with said active area region (12; 42) and said body (11), a selection bipolar transistor (20; 43; 50);

forming, on top of said body, a plurality of storage components (3), each storage component having a terminal connected to a respective conduction region (14) and defining, together with said bipolar transistor, a cell (2) of said cell array.

16. The process according to claim 15, wherein said step of forming a plurality of active area regions (12; 42) comprises:

growing insulating regions (13; 40) on said body (10), said insulating regions surrounding said active area regions (12; 42);

and implanting said active area regions with doping agents of said second conductivity type.

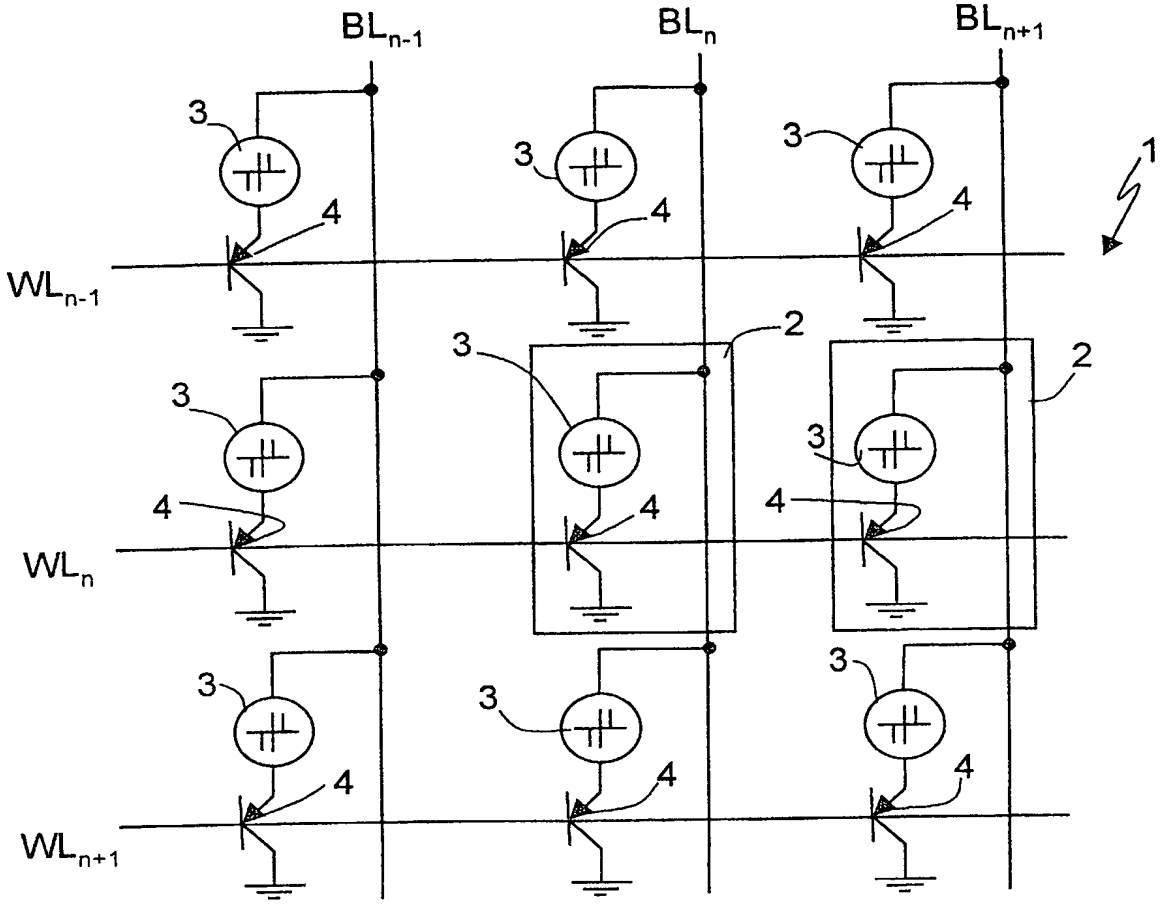
17. A process according to claim 16, wherein said insulating regions (13) and said active area regions (12) have strip-like shape.

18. A process according to claim 16, wherein said insulating regions (40) form a grid-like structure and said active area regions (43) have a rectangular shape.

ABSTRACT

A cell array (1) is formed by a plurality of cells (2) including each a selection bipolar transistor (4) and a storage component (3). The cell array is formed in a body (10) including a common collector region (11) of P type; a plurality of base regions (12) of N type, overlying the common collector region (11); a plurality of emitter regions (14) of P type formed in the base regions; and a plurality of base contact regions (15) of N type and a higher doping level than the base regions, formed in the base regions (12; 42), wherein each base region (12) is shared by at least two adjacent bipolar transistors (20).

Figures 3, 4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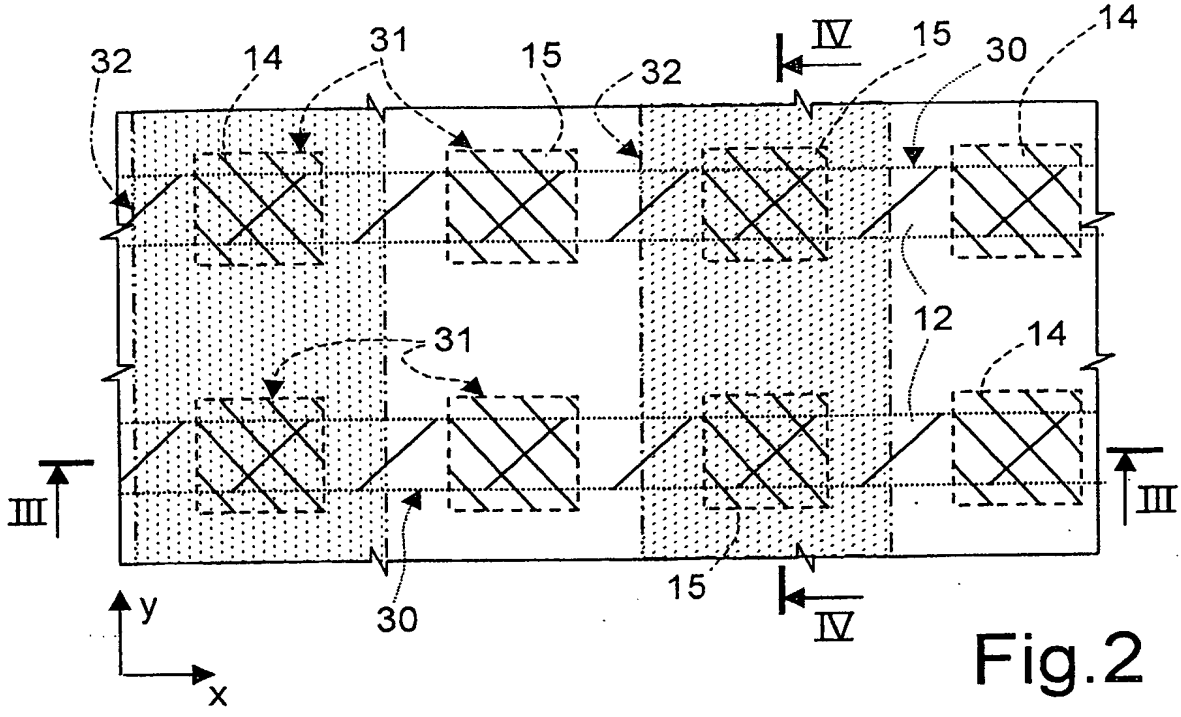
BL$_n$
BL$_{n+1}$
WL$_{n-1}$
WL$_n$
WL$_{n+1}$
1
2
3
4

Fig.1


32
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y
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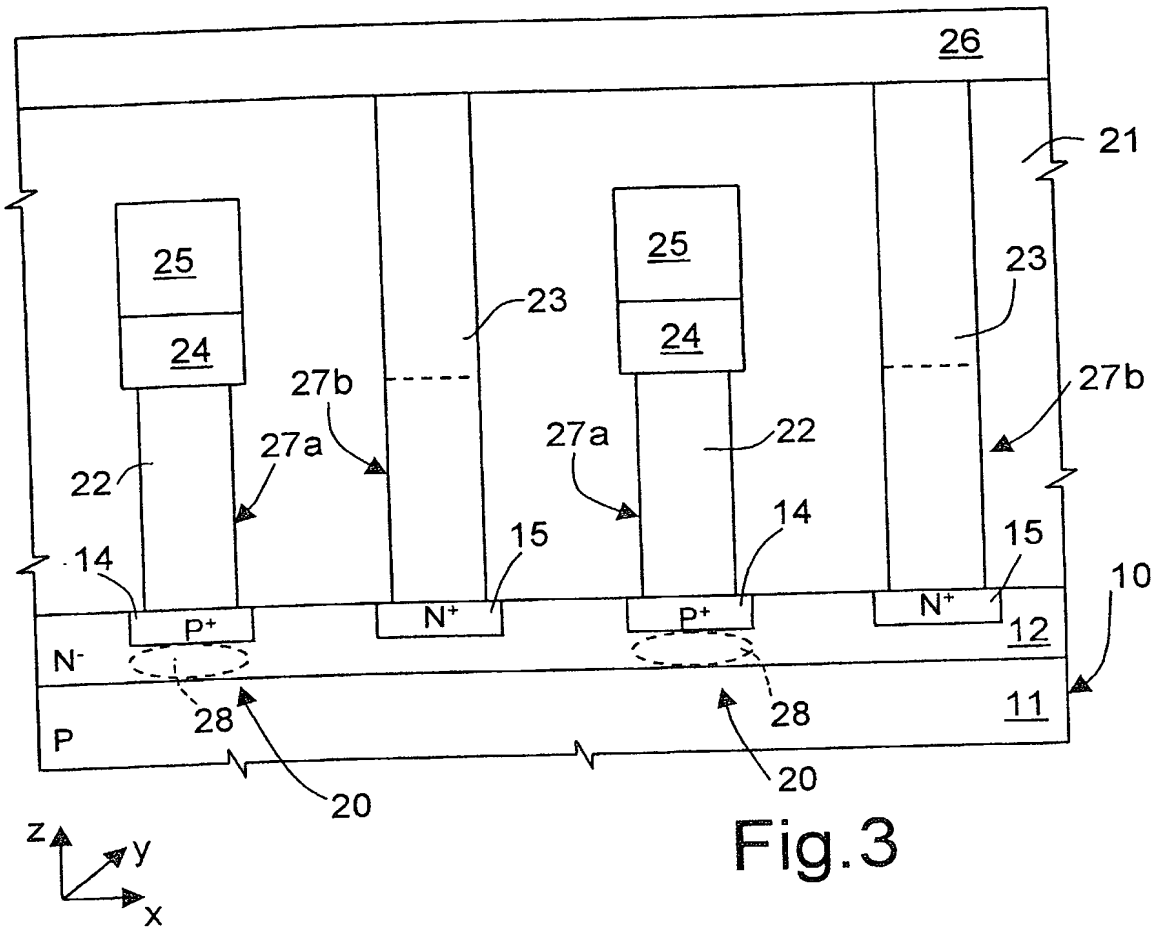
Fig.2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24
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27b
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10
P+
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z
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Fig.3

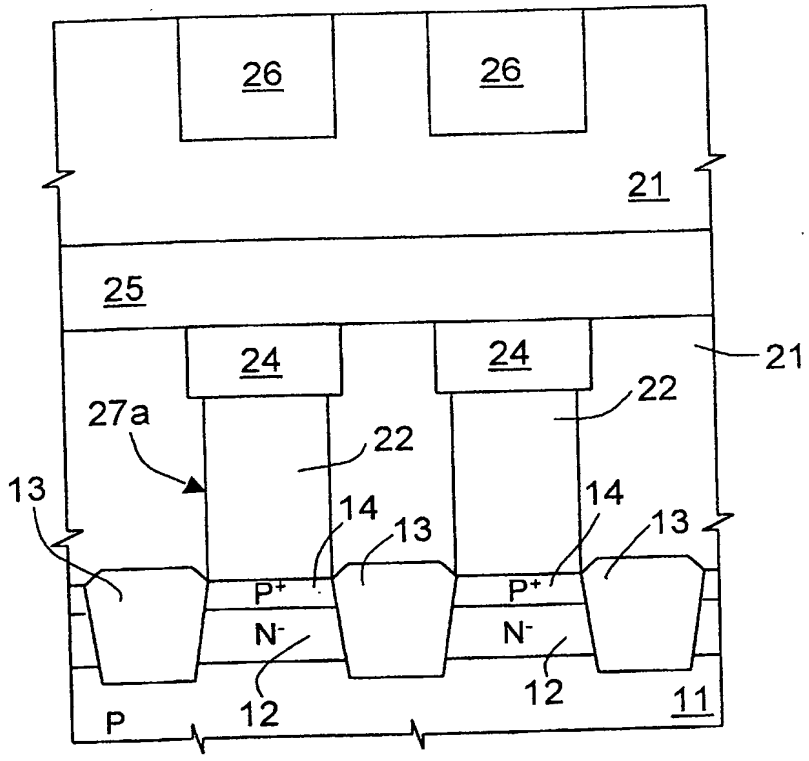
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Fig.4

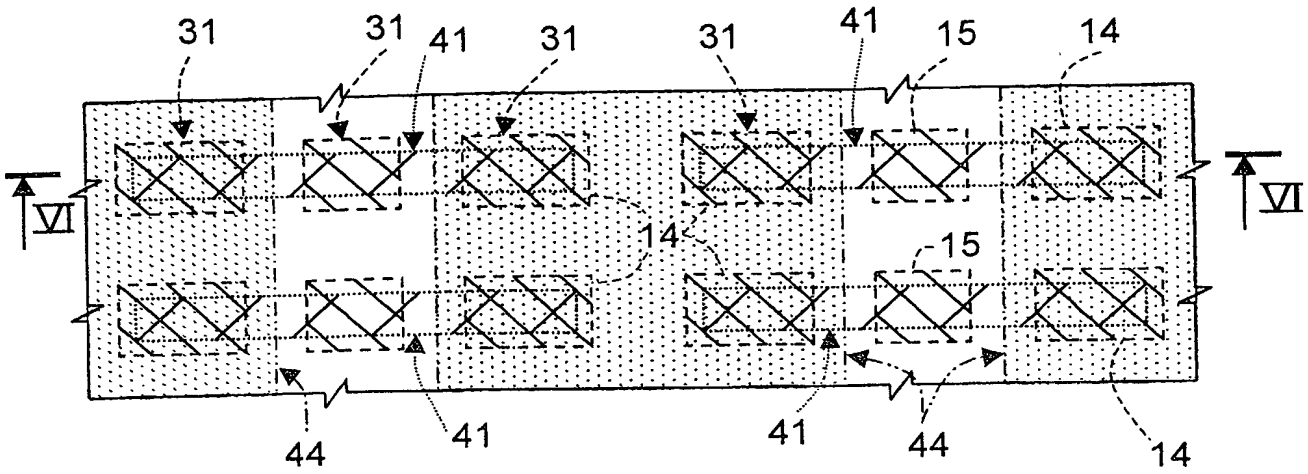
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Fig.5

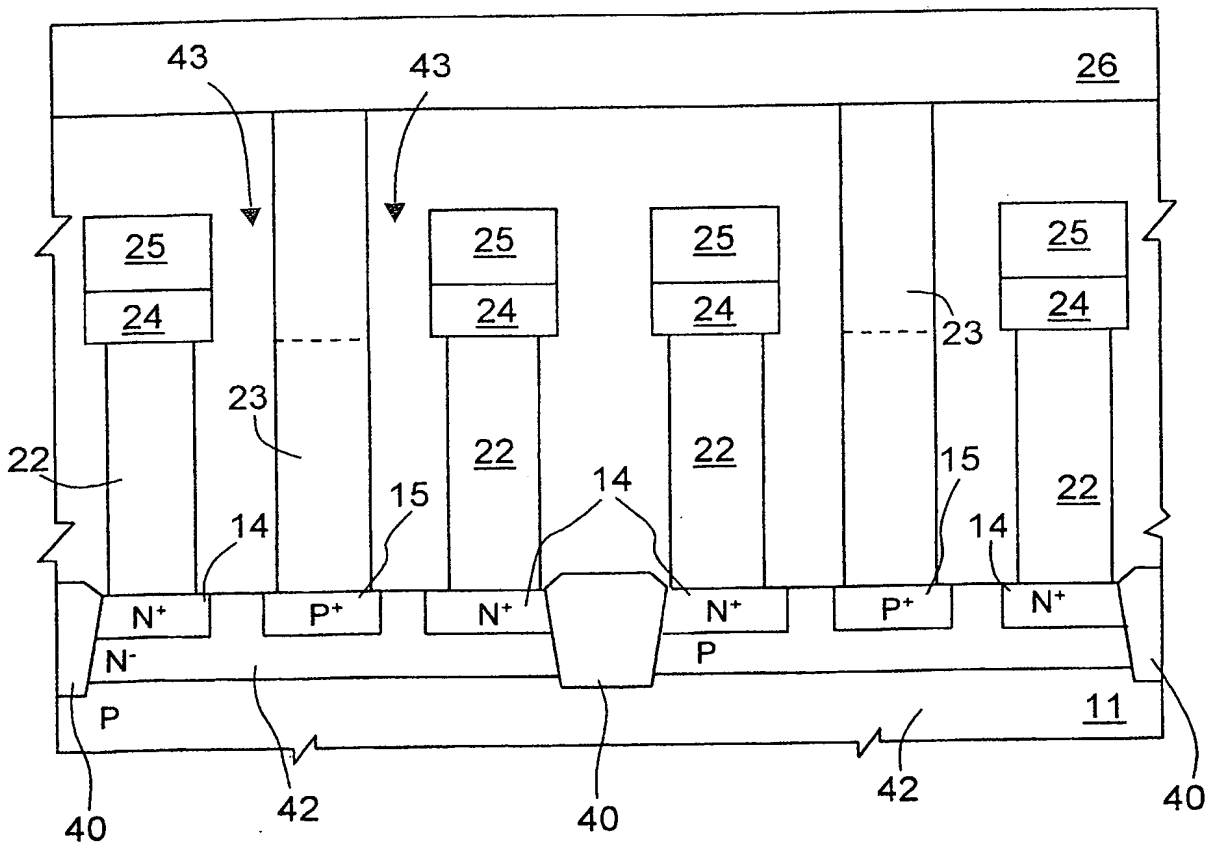
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Fig.6

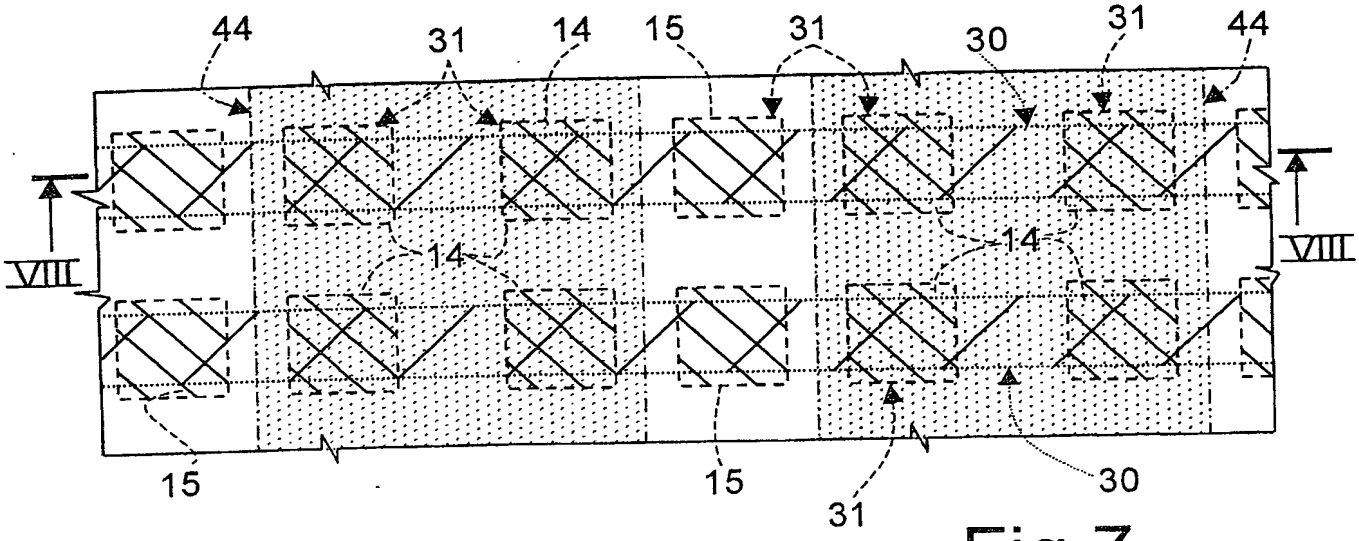
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Fig.7

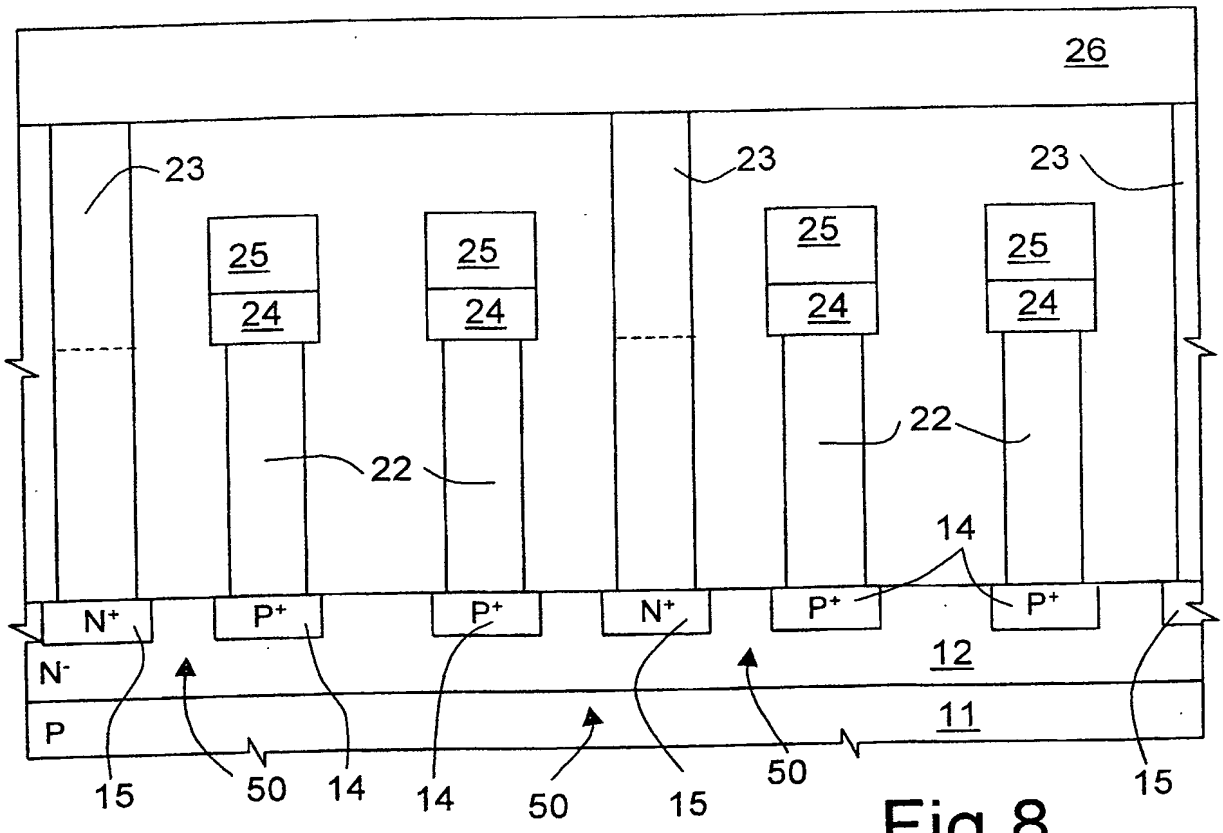
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Fig.8